DIFFERENTIAL CURRENT-MODE SENSING METHODS AND APPARATUSES FOR MEMORIES

ABSTRACT OF THE DISCLOSURE

Disclosed is a memory architecture where current sense amplifiers are used instead of voltage sense amplifiers, and where the memory cells normally disposed along a single bit line are divided between two half bit lines. Each half bit line is coupled to a respective input of the current sense amplifier. When one of the memory cells is selected for reading, it couples a current related to its stored data state to the half bit line that it is coupled to. During this operation, a reference current is generated on the other half bit line. Also disclosed are novel current sense amplifiers.